REMARKS

Claims 2 and 3 have been amended to conform with the language of independent claim 1, from which they depend. New claims 9-17 have been added to further scope the invention. No new matter has been entered by any of these amendments.

Turning to the Examiner's objection to the drawings and the Examiner's §112 rejection of claim 3 as indefinite, claim 2 has been amended to specify that a wiring pattern connects a terminal on said upper chip to a second terminal on said substrate. This feature is clearly shown in Applicant's FIG. 3, and it is believed that the Examiner's objection to the drawings and rejection of claim 3 have been overcome.

Turning to the rejection of claims 1, 2, 5, 7 and 8 under 35 USC §102 as anticipated by newly cited Hikita et al. (U.S. Patent No. 6,133,637), the Examiner's rejection is in error. Claim 1 requires that the wiring patterns are in direct contact with both a lower chip and an upper chip. In Hikita et al., FIG. 39 referred to by the Examiner, and wires W are in direct contact with wiring substrate 14 and lower substrate 17, not upper chip 16. Thus, Hikita et al. cannot anticipate claims 1, 2, 5, 7 and 8.

Turning to the rejection of claims 3, 4 and 6 under 35 USC §103 as obvious over Hikita et al. in view of newly cited Takiar et al. (U.S. Patent No. 5,495,398), claims 3, 4 and 6 are directly or indirectly dependent on claim 1. The deficiencies of Hikita et al. vis-à-vis claim 1 have been discussed above. Takiar et al. does not supply the missing teachings to achieve or render obvious claim 1 or claims 3, 4 or 6, which depend thereon. Nowhere does Takiar et al. teach an upper substrate with bonding pads located on a bonding surface. Thus, no combination of Hikita et al. and Takiar et al. can achieve or render obvious the instant claims.

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As for newly added claims 9-17, these claims are directed to the connection relationship between the upper chip, wiring sheet, lower chip and package substrate. The cited references do not teach a middle layer for connecting an upper chip and a lower chip, as required by Applicant's claims. Comparing claims 9-17 with Hikita et al., the present invention has the distinctive features that (1) a middle layer (a wiring sheet) is between an upper chip and a lower chip and (2) there is no bonding wire connecting the second layer (counting from the upper side) and the third layer.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP NON-FEE AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 29, 2004 at Tucson, Arizona.

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